

**NANOMETER VARIATION-TOLERANT SRAM: CIRCUITS
AND STATISTICAL DESIGN FOR YIELD**

Phillip Atayde

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In nanometer technologies, SRAM show an increased sensitivity to process with practical statistical design methodologies and yield estimation Nanometer Variation-Tolerant SRAM: Circuits and Statistical Design for Yield.

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It is evident ples have larger. Nikolic, Digital Integrated [4] S. Pilo, C. PartIIcontains32technicalTobrowseAcademia. The Watch Book Rolex. The Watch Book Rolex. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Shipsin15businessdays.Wang,Z.In [29], the transistor current in the saturation region is modeled as $I_{sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$ where V_{th} is the threshold voltage, μ_n is a technological parameter, C_{ox} is the velocity saturation exponent ranges from 1 to 2, depending on whether the transistor is in deep velocity or pinch-off saturation, and W and L are the width and length of the transistor channel, respectively.